Paragraph beginning at page 2, line 13:

In order to describe the testing architecture in detail, reference is made to Figs. 2A, 2B and 1A, 1B. Fig. 2A is a timing sequence of the start signal output through the conventional testing architecture in Figs. 1A and 1B. Fig. 2B is a testing flow chart of the conventional testing architecture. In step S10, the start clock signal is transmitted in sequence to the DUT 10 and the SIPO 110 by the tester to drive the DUT 10 to transmit the data in series to the SIPO 110. The corresponding time interval is tl, as seen in Fig. 2A. In time interval tl of step S11, 8 bits of the serial starting clock signal is converted into a parallel signal, and then the parallel signal is transmitted to the buffer 120. In step S12, that is, in corresponding time interval t2 in Fig. 2A, a stop signal is transmitted from the tester 130 to the DUT 10 to stop relaying the data to the SIPO 110. This is a kind of hardware time delay. The time delay can benefit the testing process.

Paragraph beginning at page 5, line 5:

Fig. 2B is a testing flow chart of the conventional testing architecture;

Paragraph beginning at page 6, line 16:

In order to describe the preferred embodiment of the invention in detail, please refer to Figs. 4A, 4B and 3. Fig. 4A is a timing sequence of the clocks output from the microprocessor 210. Fig. 4B is a testing flow chart of the preferred embodiment of the invention. In step S20, the test-starting signal is output from the result sorting and display device 220 to the microprocessor 210. In time interval tl in Fig. 4A, the clocks #1, #2, #3...are output in sequence from the

microprocessor 210 to the DUT 10, ~~as shown in Fig. 4A.~~ and the corresponding stored data is then transmitted in series from the DUT 10 to the microprocessor 210 (step S21). Here the 8 bits of data are taken as an example; therefore, there are 8 clocks in time interval tl. ~~The corresponding stored data is transmitted in series from the DUT 10 to the microprocessor 210.~~

Paragraph beginning at page 7, line 1:

In the time interval tl, serial ~~Serial~~ data output from a semiconductor memory device can be received, tested and compared by the microprocessor 210 (step S22). Therefore, data such as 8 bits of data output from the DUT 10 are tested and compared by the microprocessor 210. In time interval tl, the tested and compared results are transmitted to the result and display device 220 by the microprocessor 210. ~~After~~, and after the tested and compared results are received by the result sorting and display device 220, the tested results are sorted by the result sorting and display device 220 (step S23). Moreover, a sorted result is displayed for the benefit of the operators checking the DUT 10.

In the Drawings:

Please amend drawings of Fig. 4A according to the annotated sheet showing changes. The attached sheets include a replacement sheet and an annotated sheet.